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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,721	01/21/2004	Thomas James Fox	RPS920030082US1	3705

45503 7590 08/23/2006

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ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,721	FOX ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/24/04* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This Office Action is in response to the application 10/761,721 filed on 01/21/2004.

2. Claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 18-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 18, this claim should depend on claim 12 instead of claim 11 since claim 11 is a method claim.
As per claim 20, this claim also should depend on claim 12 instead of claim 1 since claim 1 is a method claim.
Clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in

order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKay et al. (U.S. 6,138,247 hereafter referred to as McKay) in view of Morikawa et al. (U.S. 5,898,829 hereafter referred to as Morikawa).

As per claim 1:

McKay substantially teaches the invention. McKay teaches:

- In an multiprocessor data processing system (MP), a method for dynamically providing spare processor resources when an operating processor fails (i.e., ***fail-over process)*** [abstract, fig. 10, col. 2, lines 10-30]; method comprising:

- holding-off a spare processor during a POST (power on self test), wherein said spare processor is available within said MP along with at least two operating processors, and said spare processor is not allocated any processing load by the operating system (OS) following the POST [fig. 10, col. 2, lines 10-30 and col. 3, lines 30-53];

- when one of the operating processors is determined to be failing, dynamically (i.e., ***seamless switchover***) activating said spare processor to replace the failing operating processor, wherein the processing load of the failing processor is automatically sent to the spare processor for processing (i.e., ***fail-over process)*** [abstract, fig. 10, col. 2, lines 10-30, col. 6, lines 59 through col. 7, lines 14, col. 8, lines 20-31].

McKay does not explicitly address:

- MP configured according to IA-32 architecture (i.e., system management interrupt/SMI).

However, McKay does disclose capability of:

- A multiprocessors system configured for switching (i.e., fail-over) between multiprocessors [abstract, fig. 10, col. 2, lines 10-30] comprising:

- a data connectivity among multi-processors, plurality of memory areas, selection means, switching means, system processor boards, … [fig. 1, col. 2, lines 31-47].

- ***a multi-system processor architectures including multi-configuration management function, examining and interruption enable management, , seamless switching and***

continuity operation functions [col. 2, lines 30-35, col. 7, lines 1-7, col. 8, lines 1-30]

In addition, Morikawa explicitly teaches:

- A fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising:
- an ***operational state information*** used in supporting the failover process [col. 21, lines 20-30] via a ***multi-configuration "watchdog" means*** [col. 5, lines 20-42].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing McKay's ***multi-system processor architectures including multi-configuration management function, examining and interruption enable management, , seamless switching and continuity operation functions*** as being the MP configured according to IA-32 architecture as claimed by Applicant. This is because McKay's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***fail-over***) via plurality of processors via configuration and interrupting processes. By utilizing these capabilities, the multi-data processing system can be directed or redirected

promptly and functioned properly during failover switching process in supporting the system operation; second, by applying the ***operational state information*** used in supporting the failover process via a ***multi-configuration "watchdog"*** means as taught by Morikawa in conjunction with the multiprocessors system configured for switching (i.e., fail-over) between multiprocessors as taught by McKay, the multi-processors within fault tolerant networking system including backup capability (i.e., failover) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the multi-data processors, failover, and/or fault-tolerant system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2-3:

McKay substantially teaches the invention. McKay teaches:

- In an multiprocessor data processing system (MP), a method for dynamically providing spare processor resources when an operating processor fails (i.e., ***fail-over process)*** [abstract, fig. 10, col. 2, lines 10-30]; method comprising:

- MP includes a basic input/output system (BIOS) [col. 2, lines 30-47] and a processor register linked to said BIOS, which indicates which processors among said operating processors and said spare processors are currently available to said OS for allocating load, wherein said holding off of the spare processor comprises: setting a bit within said register corresponding to each of said operating processors to an active state during said initial POST, wherein said active state indicates to said OS that the corresponding operating processor is available for allocating load; and setting a bit corresponding to said spare processor an inactive state. [fig. 10, col. 2, lines 10-30, col. 3, lines 30-53, col. 4, lines 32-50, col. 6, lines 10-35];

- wherein said dynamically activating step comprises: re-setting a bit corresponding to the failing processor to an inactive state; and setting said bit corresponding to said spare processor to an active state (i.e., ***seamless***

switchover, ***fail-over process)*** [abstract, fig. 10, col. 2, lines 10-30, col. 4, lines 30-52, col. 6, lines 10-35, col. 6, lines 59 through col. 7, lines 14, col. 8, lines 20-31].

In addition, Morikawa explicitly teaches:

- A fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising:
- an ***operational state information*** used in supporting the ***failover process*** [col. 21, lines 20-30] via a ***multi-configuration "watchdog" means*** (i.e., ***using setting bit to performing this watchdog function***) [col. 5, lines 20-42].

As per claims 4-7:

McKay further teaches:

- holding-off a spare processor during a POST (power on self test), wherein said spare processor is available within said MP along with at least two operating processors, and said spare processor is not allocated any processing load by the operating system (OS) following the POST [fig. 10, col. 2, lines 10-30 and col. 3, lines 30-53];

- configuration and BIOS [abstract, fig. 1, col. 2, lines 30-47]

- a message signaling processor failure (i.e., ***error detection and correction process***) [col. 7, lines 37-51].

McKay does not explicitly address:

- placing spare processor in a low-power, standby state during system boot

However, McKay does disclose capability of:

- A multiprocessors system configured for switching (i.e., fail-over) between multiprocessors [abstract, fig. 10, col. 2, lines 10-30] comprising:

- ***a standby/active and active/active multi-processor confinguration in supporting the fail-over process*** [col. 3, lines 32 through col. 4, lines 28].

In addition, Morikawa explicitly teaches:

- A fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising:

- an operational state information and a multi-configuration "watchdog" used in supporting the failover

process [col. 5, lines 20-42, col. 21, lines 20-30] via backup/active processors means [col. 5, lines 9-20].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to realize the combination of McKay's ***standby/active and active/active multi-processor confinguration in supporting the fail-over process and*** Morikawa's operational state information and a multi-configuration "watchdog" used in supporting the failover process via ***backup/active processors*** means do teach Applicant's limitation. This is because McKay's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***fail-over***) via processors configuring, ***swapping*** and interrupting processes. By utilizing these capabilities, the processor must be in low power mode in order to perform processor swapping procedure sot that the system can be directed or redirected promptly and functioned properly during failover switching process in supporting the system operation;.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the data processing system operation availability and memory/system performance.

As per claims 8-11:

McKay further teaches:

- driver-OS handshake operation [col. 13, lines 17-35 and col. 23, lines 30 through col. 24, line 37];

- saving a system state of each processor to memory (i.e., standby/active and active/active configuration mode states) [fig. 6-7col. 4, lines 53 through col. 5, lines 32

- swapping out the failing processor for the spare processor; updating system configuration parameters, including bus controller, memory and OS parameters, to reflect switch over to said spare processor from said failing processor [fig. 6-7, col. 4, lines 54 through col. 5, lines 46];

- restoring control to said OS once said spare processor has been activated [abstract, fig. 10, col. 2, lines 10-30, col. 6, lines 59 through col. 7, lines 14, col. 8, lines 20-31].

- enabling OS updates to an active processor lists, wherein said OS begins allocating threads previously running on said failed processor to said spare processor [abstract, fig. 10, col. 2, lines 10-30, col. 6, lines 59 through col. 7, lines 14, col. 8, lines 20-31].

McKay does not explicitly address:

- activating an SMI handler to temporarily take control of said system.

However, McKay does disclose capability of:

- A multiprocessors system configured for switching (i.e., fail-over) between multiprocessors [abstract, fig. 10, col. 2, lines 10-30] comprising:

- a data connectivity among multi-processors, plurality of memory areas, selection means, switching means, system processor boards, … [fig. 1, col. 2, lines 31-47].

- ***a multi-system processor architectures including multi-configuration management function, examining and interruption enable management, , seamless switching and continuity operation functions*** [col. 2, lines 30-35, col. 7, lines 1-7, col. 8, lines 1-30].

In addition, Morikawa explicitly teaches:

- A fault tolerant computer system including active/backup multi-processors failure detection and correction [abstract, fig. 6, col. 1, claims 10-20] comprising:

- an ***operational state information*** used in supporting the failover process [col. 21, lines 20-30] via a ***multi-configuration "watchdog" means*** [col. 5, lines 20-42].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing McKay's ***multi-system processor architectures including multi-configuration management function, examining and interruption enable management, , seamless switching and continuity operation functions*** as being the activating an SMI handler to temporarily take control of said system as claimed by Applicant. This is because McKay's mutli-data processors /fault tolerant system explicitly performed data failure detection and recovery (i.e., ***fail-over***) via plurality of processors via configuration and interrupting processes. By utilizing these capabilities, the multi-data processing system can be directed or redirected promptly and functioned properly during failover switching process in supporting the system operation; second, by applying the ***operational state information*** used in supporting the failover process via a ***multi-configuration "watchdog"*** means as taught by Morikawa in conjunction with the multiprocessors system configured for switching (i.e., fail-over) between multiprocessors as taught by McKay, the multi-processors within

fault tolerant networking system including backup capability (i.e., failover) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its state information functionality for the same reasons set forth as described in claim 1, **supra**.

As per claims 12-23:

Due to the similarity of claims 12-23 to claims 1-11 except for a multiprocessor data processing system comprising ***means*** for holding-off the spare processor during POST, ***means*** for dynamically activating spare processor, ***means*** for setting a bit within register, ***means*** for resetting a bit, etc… instead of a ***method*** comprising a multiprocessor data processing system comprising holding-off the spare processor during POST, dynamically activating spare processor, setting a bit within register, resetting a bit, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-11. **In addition, all of the limitations have been noted in the rejection as per claims** 1-11. Such as, However, McKay explicitly disclose a multiprocessors system configured for switching (i.e., fail-over) between multiprocessors [abstract, fig. 10, col. 2, lines 10-30] comprising ***a data connectivity among multi-***

processors, plurality of memory areas, selection means, switching means, multi-system processor boards, … [fig. 1, col. 2, lines 31-47].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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